WHAT IS CLAIMED IS:

1. A semiconductor light emitting device comprising:

a semiconductor substrate,

an active region comprising a strained quantum well layer, and

a cladding layer for confining carriers and light emissions,

wherein an amount of lattice strains in said quantum well layer is in excess of 2% against either said semiconductor substrate or said cladding layer.

2. The semiconductor light emitting device according to claim 1, wherein a thickness of said quantum well layer is in excess of a critical thickness calculated by a relationship of Matthews and Blakeslee.

3. The semiconductor light emitting device according to claim 1, wherein said semiconductor substrate is composed of GaAs.

4. The semiconductor light emitting device according to claim 1, wherein said strained quantum well layer is composed

of $Ga_x In_{1-x} N_y As_{1-y}$ ($0 \leq x \leq 1, 0 \leq y < 1$).

5. The semiconductor light emitting device according to claim 4, wherein said strained quantum well layer composed of $Ga_x In_{1-x} N_y As_{1-y}$ ($0 \leq x \leq 1, 0 \leq y < 1$) is characterized to have a photoluminescence peak wavelength of at least 1.12 micron for GaInAs ($y=0$).

6. The semiconductor light emitting device according to claim 4, wherein the In content in said strained quantum well layer is at least 30% of group-III elements included therein.

7. The semiconductor light emitting device according to claim 4, wherein the N content in said strained quantum well layer is from 0% to 1% of group-V elements included therein.

8. The semiconductor light emitting device according to claim 1, wherein a plane orientation of said semiconductor substrate is in a (100) direction with an allowable deviation of at most 5°.

9. The semiconductor light emitting device according to claim 1, wherein said cladding layer is composed of either

GaInP or GaInPAs.

10. The semiconductor light emitting device according to claim 1, further comprising a barrier layer provided in a vicinity of said strained quantum well layer to relax the strains therein.

11. The semiconductor light emitting device according to claim 1, wherein said semiconductor light emitting device is a surface emitting type device.

12. The semiconductor light emitting device according to claim 11, further comprising:

a first mirror region formed adjacent to said semiconductor substrate, a quantum well active region formed thereon, comprising said strained quantum well layer; and

a second mirror region formed on an opposite side of said active region from said first mirror region, to collectively constitute an optical cavity for achieving stimulated light emissions,

wherein at least said first mirror region is constructed to have a periodic multi-layered structure of thin semiconductor layers with alternating higher and lower

refractive indices.

13. The semiconductor light emitting device according to claim 11, further comprising:

a first mirror region formed adjacent to said semiconductor substrate, a quantum well active region formed thereon, comprising said strained quantum well layer; and

a second mirror region formed on an opposite side of said active region from said first mirror region, to collectively constitute an optical cavity for achieving stimulated light emissions,

wherein at least said first mirror region is constructed to have a periodic multi-layered structure of thin semiconductor layers with alternating higher and lower refractive indices, in which said thin semiconductor layers are characterized as to contain no Al.

14. The semiconductor light emitting device according to claim 11, further comprising;

a first mirror region formed adjacent to said semiconductor substrate, a quantum well active region formed thereon, comprising said strained quantum well layer; and

a second mirror region formed on an opposite side of said

active region from said first mirror region, to collectively constitute an optical cavity for achieving stimulated light emissions,

wherein at least said first mirror region is constructed to have a periodic multi-layered structure of thin dielectric layers with alternating higher and lower refractive indices.

15. The semiconductor light emitting device according to claim 1, wherein said strained quantum well layer is formed at temperatures of at most 600° C.

16. The semiconductor light emitting device according to claim 1, wherein said light emitting device comprises III-V alloy semiconductor layers formed by metal organic chemical vapor deposition (MOCVD) using organic compounds as the source material for the III-group elements.

17. The semiconductor light emitting device according to claim 1, wherein said strained quantum well layer is formed using nitrogen containing organic compounds selected from the group consisting of dimethylhydrazine and monomethylhydrazine.

18. A semiconductor light emitting device comprising:

a semiconductor substrate,

an active region comprising a strained quantum well layer, and

a cladding layer for confining carriers and light emissions,

wherein a thickness of said quantum well layer is in excess of critical thickness calculated by a relationship of Matthews and Blakeslee.

19. The semiconductor light emitting device according to claim 18,

wherein an amount of lattice strains in said quantum well layer is in excess of 2% against either said semiconductor substrate or said cladding layer.

20. The semiconductor light emitting device according to claim 18, wherein said semiconductor substrate is composed of GaAs.

21. The semiconductor light emitting device according to claim 18, wherein said strained quantum well layer is composed of $Ga_x In_{1-x} N_y As_{1-y}$ $(0 \leq x \leq 1, 0 \leq y < 1)$.

22. The semiconductor light emitting device according to claim 21, wherein said strained quantum well layer composed of $Ga_x In_{1-x} N_y As_{1-y}$ $(0 \leq x \leq 1, 0 \leq y < 1)$ has a photoluminescence peak wavelength of at least 1.12 micron for GaInAs (y=0).

23. The semiconductor light emitting device according to claim 21, wherein the In content in said strained quantum well layer is at least 30% of group-III elements included therein.

24. The semiconductor light emitting device according to claim 21, wherein the N content in said strained quantum well layer is from 0% to 1% of group-V elements included therein.

25. The semiconductor light emitting device according to claim 18, wherein a plane orientation of said semiconductor substrate is in a (100) direction with an allowable deviation of at most 5°.

26. The semiconductor light emitting device according to claim 18, said cladding layer is composed of either GaInP or GaInPAs.

27. The semiconductor light emitting device according to

claim 18, further comprising a barrier layer provided in a vicinity of said strained quantum well layer to relax a strains therein.

28. The semiconductor light emitting device according to claim 18, wherein said semiconductor light emitting device is a surface emitting type device.

29. The semiconductor light emitting device according to claim 28, further comprising:

a first mirror region formed adjacent to said semiconductor substrate, a quantum well active region formed thereon, comprising said strained quantum well layer; and

a second mirror region formed on an opposite side of said active region from said first mirror region, to collectively constitute an optical cavity for achieving stimulated light emissions,

wherein at least said first mirror region is constructed to have a periodic multi-layered structure of thin semiconductor layers with alternating higher and lower refractive indices.

30. The semiconductor light emitting device according to

claim 28, further comprising:

a first mirror region formed adjacent to said semiconductor substrate, a quantum well active region formed thereon, comprising said strained quantum well layer; and

a second mirror region formed on an opposite side of said active region from said first mirror region, to collectively constitute an optical cavity for achieving stimulated light emissions,

wherein at least said first mirror region is constructed to have a periodic multi-layered structure of thin semiconductor layers with alternating higher and lower refractive indices, in which said thin semiconductor layers are characterized as to contain no Al.

31. The semiconductor light emitting device according to claim 28, further comprising:

a first mirror region formed adjacent to said semiconductor substrate, a quantum well active region formed thereon, comprising said strained quantum well layer; and

a second mirror region formed on an opposite side of said active region from said first mirror region, to collectively constitute an optical cavity for achieving stimulated light emissions;

wherein at least said first mirror region is constructed to have a periodic multi-layered structure of thin dielectric layers with alternating higher and lower refractive indices.

32. The semiconductor light emitting device according to claim 18, wherein said strained quantum well layer is formed at temperatures of at most 600° C.

33. The semiconductor light emitting device according to claim 18, wherein said III-V alloy semiconductor layer is formed by metal organic chemical vapor deposition (MOCVD) using organic compounds as the source material for the III-group elements.

34. The semiconductor light emitting device according to claim 18, wherein said strained quantum well layer is formed using nitrogen containing organic compounds selected from the group consisting of dimethylhydrazine and monomethylhydrazine.

35. A method of fabricating semiconductor light emitting device comprising III -V alloy semiconductor layers formed on a semiconductor substrate, such as an active region comprising a strained quantum well layer, and a cladding layer for

confining carriers and light emissions, said method comprising the step of forming said strained quantum well layer at 600° C at most.

36. The method of fabricating semiconductor light emitting device according to claim 35,

wherein said III -V alloy semiconductor layers are formed by metal organic chemical vapor deposition (MOCVD) using organometallic compounds as the source materials for the group-III elements.

37. The method of fabricating semiconductor light emitting device according to claim 35, wherein said strained quantum well layer is composed of $Ga_x In_{1-x} N_y As_{1-y}$ $(0 \leq x \leq 1, 0 \leq y < 1)$, and said at least one $Ga_x In_{1-x} N_y As_{1-y}$ $(0 \leq x \leq 1, 0 \leq y < 1)$ strained quantum well layer is formed using nitrogen containing organic compounds selected from the group consisting of dimethylhydrazine and monomethylhydrazine.

38. A semiconductor light emitting device comprising:

a semiconductor substrate, an active layer, and a cladding layer for confining carriers and light emissions,

wherein said active layer includes a III-V semiconductor

alloy containing at least Al as one group- III element and both N and As as group-V elements.

39. The semiconductor light emitting device according to claim 38, wherein said III-V semiconductor alloy has a composition of either $Al_x Ga_y In_{1-x-y} N_z As_{1-z}$ ($0<x<1, 0<y<1$) or $Al_x In_{1-x} N_y P_z As_{1-y-z}$ ($0<x<1$, $0<y<1, 0\leq z<1$).

40. The semiconductor light emitting device according to claim 38, wherein said active layer is surrounded by a structure either having no Al content or Al content less than that in said active layer.

41. The semiconductor light emitting device according to claim 38,

wherein said active layer is formed by metal organic chemical vapor deposition (MOCVD) using organometallic compounds selected from the group consisting of trimethylaluminum and trimethylaluminum, as the Al source.

42. The semiconductor light emitting device according to claim 38,

wherein said active layer is formed by metal organic

chemical vapor deposition (MOCVD) using organometallic compounds selected from the group consisting of dimethylhydrazine and monomethylhydrazine, as the N source.

43. A method of fabricating a light emitting device comprising III -V alloy semiconductor layers,

said method comprising the step of depositing said III -V alloy semiconductor layers by metal organic chemical vapor deposition (MOCVD) using organometallic compounds selected from the group consisting of trimethylaluminum and trimethylaluminum, as the Al source.

44. The method of fabricating a light emitting device according to claim 43,

further comprising the step of depositing said III -V alloy semiconductor layers by metal organic chemical vapor deposition (MOCVD) using organometallic compounds selected from the group consisting of dimethylhydrazine and monomethylhydrazine, as the N source.

45. The semiconductor light emitting device according to claim 1, wherein said strained quantum well layer includes at least Ga, In, N and As.

46. The semiconductor light emitting device according to claim 1, wherein said semiconductor substrate is composed of InP, and wherein said strained quantum well layer is composed of a material selected from the group consisting of GaInAs, GaInPAs, InPAs and InNPAs.

47. The semiconductor light emitting device according to claim 18, wherein said strained quantum well layer includes at least Ga, In, N and As.

48. The semiconductor light emitting device according to claim 18, wherein said semiconductor substrate is composed of InP, and wherein said strained quantum well layer is composed of a material selected from the group consisting of GaInAs, GaInPAs, InPAs and InNPAs.

49. A semiconductor light emitting device comprising:

a semiconductor substrate, and

an active region comprising a strained quantum well layer, wherein the amount of lattice strains in said quantum well layer is in excess of 2% against either said semiconductor substrate or said cladding layer.

50. The semiconductor light emitting device according to claim 49, wherein the thickness of said quantum well layer is in excess of the critical thickness calculated by the relationship of Matthews and Blakeslee.

51. The semiconductor light emitting device according to claim 49, wherein said semiconductor substrate is composed of GaAs.

52. The semiconductor light emitting device according to claim 49, wherein said strained quantum well layer is composed of $Ga_x In_{1-x} N_y As_{1-y}$ ($0 \leq x \leq 1, 0 \leq y < 1$).

53. The semiconductor light emitting device according to claim 52, wherein said at least one strained quantum well layer composed of $Ga_x In_{1-x} N_y As_{1-y}$ ($0 \leq x \leq 1, 0 \leq y < 1$) is characterized to have a photoluminescence peak wavelength. of at least 1.12 micron for GaInAs ($y=0$).

54. The semiconductor light emitting device according to claim 52, wherein the In content in said strained quantum well layer is at least 30% of group-III elements included therein.

55. The semiconductor light emitting device according to claim 52, wherein the N content in said strained quantum well layer is from 0% to 1% of group-V elements included therein.

56. The semiconductor light emitting device according to claim 49, wherein the plane orientation of said semiconductor substrate is in the (100) direction with the allowable deviation of at most 5°.

57. The semiconductor light emitting device according to claim 49, wherein said strained quantum well layer includes at least Ga, In, N and As.

58. The semiconductor light emitting device according to claim 49, wherein said strained quantum well layer is composed of a material selected from the group consisting of GaInAs, GaInPAs, InPAs and InNPAs.

59. A semiconductor light emitting device comprising:

a semiconductor substrate, and

an active region comprising a strained quantum well layer,

wherein the thickness of said quantum well layer is in

excess of the critical thickness calculated by the relationship of Matthews and Blakeslee.

60. The semiconductor light emitting device according to claim 59, wherein the amount of lattice strains in said quantum well layer is in excess of 2% against either said semiconductor substrate or said cladding layer.

61. The semiconductor light emitting device according to claim 59, wherein said semiconductor substrate is composed of GaAs.

62. The semiconductor light emitting device according to claim 59, wherein said at least one strained quantum well layer is composed of $Ga_x In_{1-x} N_y As_{1-y}$ ($0 \leq x \leq 1, 0 \leq y < 1$).

63. The semiconductor light emitting device according to claim 62, wherein said at least one strained quantum well layer composed of $Ga_x In_{1-x} N_y As_{1-y}$ ($0 \leq x \leq 1, 0 \leq y < 1$) is characterized to have a photoluminescence peak wavelength of at least 1.12 micron for GaInAs ($y=0$).

64. The semiconductor light emitting device according to

claim 62, wherein the In content in said at least one strained quantum well layer is at least 30% of group-III elements included therein.

65. The semiconductor light emitting device according to claim 62 wherein the N content in said at least one strained quantum well layer is from 0%, to 1% of group-V elements included therein.

66. The semiconductor light emitting device according to claim 59, wherein the plane orientation of said semiconductor substrate is in the (100) direction with the allowable deviation of at most 5°.

67. The semiconductor light emitting device according to claim 59, wherein said strained quantum well layer includes at least Ga, In, N and As.

68. The semiconductor light. emitting device according to claim 59, wherein said strained quantum well layer is composed of a material selected from the group consisting of GaInAs, GaInPAs, InPAs and InNPAs.

69. The semiconductor light emitting device according to claim 1, wherein said cladding layer is formed at temperatures of at most 780° C following a formation of said active region.

70. An optical transmission module,

said module comprising:

a semiconductor light emitting device,

wherein said semiconductor light emitting device is as claimed in any one of claims 1 through 17.

71. An optical transmitter receiver module,

said module comprising:

a semiconductor light emitting device,

wherein said semiconductor light emitting device is as claimed in any one of claims 1 through 17.

72. An optical communication system,

said system comprising:

a semiconductor light emitting device,

wherein said semiconductor light emitting device is as claimed in any one of claims 1 through 17.

73. A computer system incorporating an optical

communication system,

said communication system comprising:

a semiconductor light emitting device,

wherein said semiconductor light emitting device is as claimed in any one of claims 1 through 17.

74. A network system incorporating an optical communication system,

said communication system comprising:

a semiconductor light emitting device,

wherein said semiconductor light emitting device is as claimed in any one of claims 1 through 17.